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Void-Free Direct Bonding of CMUT Arrays with Single Crystalline Plates and Pull-In Insulation

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Abstract*—The implications on direct bonding quality, when using a double oxidation step to fabricate capacitive micromachined ultrasonic transducers (CMUTs), is analyzed. The protrusions along the CMUT cavity edges created during the second oxidation are investigated using simulations, AFM measurements, and a proposed analytical model, which is in good agreement with the simulated results. The results demonstrate protrusion heights in the order of 10 nm to 40 nm, with higher oxidation temperatures giving the highest protrusions. Isotropically wet etched cavities exhibit significantly smaller protrusions than anisotropically plasma etched cavities after the second oxidation. It is demonstrated that the protrusions will prevent good wafer bonding without subsequent polishing or etching steps. A new fabrication process is therefore proposed, allowing protrusion-free bonding surfaces with no alteration of the final structure and no additional fabrication steps compared to the double oxidation process. Two identical CMUT arrays with circular and square cavities having diameter/side lengths of 72 µm/65 µm and a 20 µm interdistance are fabricated with the two processes, demonstrating void-free bonding and 100 % yield from the proposed process compared to poor bonding and 7 % yield using the double oxidation process.

I. Introduction

Capacitive micromachined ultrasonic transducers (CMUTs) fabricated using direct wafer bonding offers various advantages such as single crystalline plates with a well-defined thickness and highly predictable mechanical properties. Huang et al. demonstrated a simple fabrication process where the CMUTs are made by etching out cavities in a grown oxide on a silicon wafer. This wafer is bonded to a silicon-on-insulator (SOI) wafer, which after removal of the handle and the buried oxide defines the plate/top electrode [1]. An insulation oxide in the bottom of the cavity is typically grown through a second oxidation after the cavity etch to prevent short circuiting during pull-in and avoid leak currents due to contaminations in the cavities [1], [2]. However, this process creates protrusions at the edge of the cavity as demonstrated in Fig. 1a.

In this paper, the height of the protrusions originating from a double oxidation for various processing parameters is investigated through simulations, analytical estimates, and AFM measurements. It is concluded that, for the investigated processing parameters, the prostrusions are of such a height that direct wafer bonding of a typical CMUT array is impaired or completely prohibited if subsequent etching or grinding steps are not introduced to planarize the bonding surfaces. An alternative simple fabrication approach is therefore proposed, where the cavities are etched in an oxide grown on the SOI wafer. The insulation oxide is then grown on a second wafer, and the two wafers are bonded by SiO_2/SiO_2 direct bonding, see Fig. 1b. Without introducing further processing steps, this provides protrusion-free bonding surfaces and thus optimal conditions for direct bonding. The superiority of the proposed process is demonstrated in practice by fabricating CMUT arrays with typical dimensions using both methods, showing poor bonding results for the non-planarized double oxidation process and void-free bonding results for the proposed process.

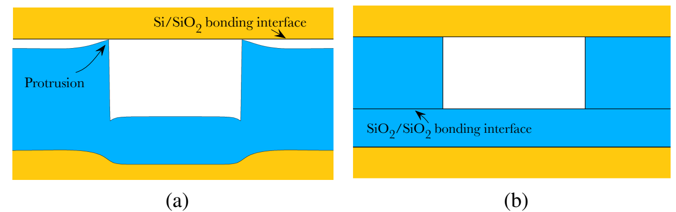

Fig. 1: Cross-sectional views of the CMUT cavities in the two different fabrication approaches. (a) Double oxidation process. (b) The proposed process. Si is orange and SiO_2 is blue.

II. Methods and Materials

A. Protrusion Investigations

The protrusion height was investigated experimentally as a function of processing parameters through two individual oxidations aiming for a 350 nm and a 200 nm oxide layer, respectively. The latter was achieved through various oxidation approaches as described below. The two oxide thicknesses were chosen as they represent realistic values for a typical CMUT design. The first oxidation was performed on six 500 µm single side polished n-type ⟨100⟩ 4” silicon wafers with a resistivity of 1-10 Ωcm, and the oxide thickness was measured to be 357 ± 1 nm. A lithography step on each wafer was followed by a cavity etch, defining square arrays of circular cavities with a diameter of 72 µm and an interspacing of 20 µm distributed over the entire wafer. In order to investigate the effect of anisotropically and isotropically etched cavities, two different etches were used to etch out cavities in the oxide; on the first three of the wafers, an

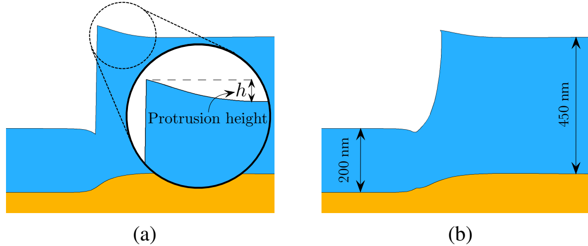

Fig. 2: Simulated cavity profile after the second oxidation in (a) an anisotropically etched cavity and (b) an isotropically etched cavity. Si is orange and SiO_2 is blue.

anisotropic reactive ion etch was used, while the remaining three were subjected to a buffered hydrogen flouride (HF) wet etch. Reference values of the protrusion height were measured with atomic force microscopy (AFM) on both an isotropically and an anisotropically etched wafer after this step. Subsequently, the wafers were cleaved in two parts, enabling six independent oxidations: Dry and wet oxidations at 950 °C and 1000 °C, and only dry at 1050 °C, and 1100 °C. In all oxidations, both an anisotropically and an isotropically etched wafer were included. Each of these second oxidations aimed for a 200 nm thick oxide in the cavities, and were all within 9 nm of this target. AFM measurements of the protrusion height were then performed on these 12 half wafers. All AFM measurements were made in tapping mode, scanning a 5 µm by 5 µm area covering the cavity edge. The scan direction was towards the cavity to avoid measurement artifacts such as overshooting from the abrupt step at the cavity edge. All heights reported in this study were averaged over three such measurements taken on three different cavities, each being evaluated by averaging over the 5 µm range. The measurement error bars were calculated as 2 sample standard deviations. All dry oxidations were carried out at an ambient pressure of 1 atm, while the wet oxidations were carried out at 0.85 atm as a consequence of the furnace settings.

The simulations were carried out in Athena 5.20.0.R by Silvaco Inc. using the same oxidation parameters in terms of type, final oxide thickness, temperature and pressure as were used in the experiments. A grid size of 1 nm in the vicinity of the oxide cavity edge was used, growing linearly to 500 nm 5 µm from the cavity edge. The simulations were carried out using different models that either includes or excludes stress effects. All simulated results were seen to be identical in the different models, indicating negligible stress effects, and only one set of results is therefore reported in this work.

B. Array Fabrication

For the fabrication of the CMUT arrays, the double oxidation process and the proposed process were carried out on two separate pairs of bonded wafers, one for each process. The main process steps are listed in Table I. As can be seen, the two approaches share the number, order and type of process steps. The only difference is that the respective

TABLE I: A list of the main process steps used in both fabrication approaches. For each step, the wafer on which the process step is carried out in the respective approach is given.

Step	Double oxidation	Proposed process
403 nm oxidation	Standard	SOI
Lithography	Standard	SOI
Cavity etch	Standard	SOI
195 nm oxidation	Standard	Standard
Bonding	Standard/SOI	Standard/SOI
Handle removal	SOI	SOI

process steps were carried out on either a standard, 500 µm single side polished 1-10 Ωcm n-type $\langle 100 \rangle$ 4" silicon wafer or an SOI wafer with the same specifications along with a 2 µm low resistivity device layer and a buried oxide (BOX) layer of 1 µm. The lithography was performed through the same mask for both processes, containing arrays with circular and square cavities having diameter/side lengths of 72 µm/65 µm, respectively. The cavities were separated by 20 µm in regular square lattice arrays with either 324, 2304, or 9216 cavities per array, corresponding to 9 CMUT cells per element in 6×6, 16×16 and 32×32 arrays designed for a nominal resonance frequency in immersion of 3 MHz. The individual arrays were separated by 2.2 mm. The cavity etch was performed in a STI Pegasus reactive ion etcher, and the direct wafer bonding step was carried out at 50 °C, 10^{-3} mbar ambient pressure and 1500 N piston force for 5 minutes. Post-annealing was carried out in an inert nitrogen atmosphere at 1100 °C for 70 minutes [3]. Prior to both oxidations and the bonding step, the wafers were cleaned using a standard RCA cleaning procedure. Before the bonding step, the final HF dip in the RCA cleaning procedure was omitted to avoid oxide removal. After bonding, the bonded wafers were dipped in buffered HF for 10 minutes to remove the oxide from the exposed wafer surfaces, and the SOI handle was subsequently removed in an isotropic 40 minute deep reactive ion etch. After this step, only the 2 µm device layer and the 1 µm BOX layer of the SOI wafer remained, thereby clearly exposing any unbonded regions [4]. As only the bonding step was of interest to this study, the subsequent lithography and top electrode etch steps required to complete the CMUT arrays were not performed.

III. Results and Discussion

A. Protrusion Investigations

In Fig. 3, the measured protrusion heights are shown as a function of temperature. For each temperature, both wet and dry oxidation results are shown for both anisotropically and isotropically etched cavities. No measurements are given for wet oxidations at 1050 °C and 1100 °C as the required oxidation time to reach 200 nm is impractically short. Note that the simulations predict higher protrusions than the measured in most cases, the deviation being 7 nm at the most. Yet, both simulations and measurements agree on the general parameter dependency. It is thus seen that the oxidation temperature only has a minor effect on the protrusion height, with a

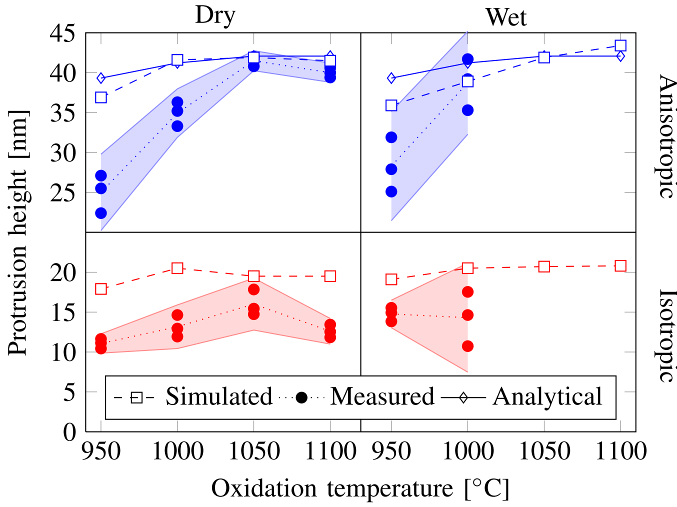

Fig. 3: Simulated, calculated and measured protrusion heights for four independent processing parameters shown as a function of oxidation temperature. The shaded areas denote a confidence interval of two standard deviations.

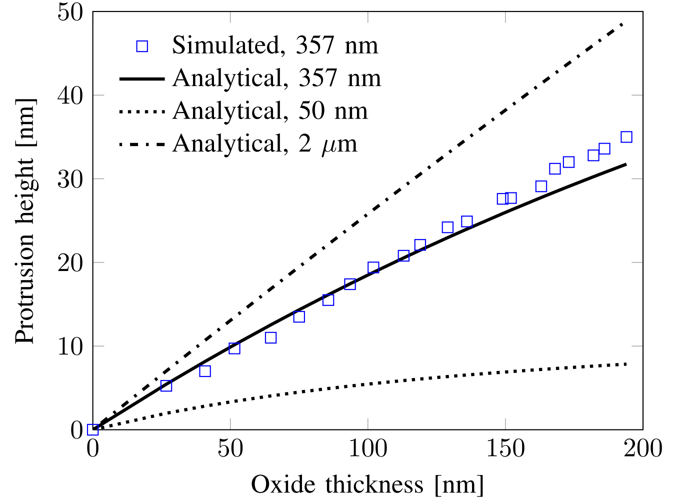

Fig. 4: Protrusion height plotted as a function of the thickness of the second oxide for three different values of the initial oxide thickness. For one of the initial oxide thicknesses, the corresponding simulated values are given.

slightly increasing protrusion height for higher temperatures. The results for the wet and dry oxidation are not significantly different, and no conclusions can be made in this case based on the measurements. A much larger effect is seen for the etch type, where the isotropically etched cavities exhibit a significantly smaller protrusion height than the anisotropically etched cavities. For all temperatures, the protrusion height is decreased by almost a factor of two. This can be explained by considering Figs. 2a and 2b, showing the simulation results of both an anisotropically (Fig. 2a) and an isotropically (Fig. 2b) etched cavity after the second oxidation. Since the isotropic etch results in a cavity edge which is retracted slightly from the beginning of the oxide masking, the edge is consequently raised less than the corresponding anisotropic case, where the cavity edge step is more abrupt. This therefore yields smaller protrusions for the isotropically etched cavities.

In the case of anisotropically etched cavities, the protrusion height can be quite accurately estimated using simple analytical considerations. Analytical models of the related LOCOS oxidation are known, but these are based on fitted parameters using nitride diffusion masks and are therefore not directly applicable to the present case [5]. According to the Deal-Grove model, the oxide growth rate is $\mathrm{d}x/\mathrm{d}t = kC/N$, where x is the oxide thickness, k the interface reaction rate constant, N the number of oxidizer molecules incorporated per unit volume of oxide, and C the concentration of oxidizer molecules at the oxide/silicon interface [6]. The interface concentration results from diffusion of the oxidizer from the gas/oxide interface where the oxidizer concentration is assumed contant. Since the oxide thickness varies due to the etched cavity, the interface concentration C is a function of position with well known values far from the cavity edge. At the mask edge, the concentration may be obtained by a full 2-D simulation, but a fair estimate is the average of the two known values $C_{\mathrm{edge}} \simeq (C_{\mathrm{c}} + C_{\mathrm{ox}})/2$, where C_{c} is the concentration in the cavity and C_{ox} the concentration at the oxide far from the cavity. As a result of that simple assumption,

$$\frac{\mathrm{d}x_{\mathrm{edge}}}{\mathrm{d}t} = \frac{1}{2}\left(\frac{\mathrm{d}x_{\mathrm{c}}}{\mathrm{d}t} + \frac{\mathrm{d}x_{\mathrm{ox}}}{\mathrm{d}t}\right) .$$

By subtracting $\mathrm{d}x_{\mathrm{ox}}/\mathrm{d}t$, integrating, and accounting for the volume expansion by a factor of 2.2 of the growing oxide compared to the consumed silicon, the protrusion height becomes

$$h = \frac{2.2 - 1}{2.2}\frac{1}{2}(\Delta x_{\mathrm{c}} - \Delta x_{\mathrm{ox}}) ,$$

where the grown oxide in the cavity and at the initial oxide, Δx_{c} and Δx_{ox}, are found using the Deal-Grove model for thermal oxidation [6].

The analytical model has been used to predict the protrusion height for the anisotropically etched cavities, and is given in Fig. 3. Only anisotropically etched cavities are considered, as the model assumes an abrupt step. The model shows good agreement with the simulations, confirming that the protrusions arise due to purely geometrical effects resulting in spatially dependent diffusant concentrations. As the study in Fig. 3 is restricted to a fixed oxide thickness, the model has also been used to plot the protrusion height as a function of the second oxide thickness for three different initial oxide thicknesses grown in a dry oxidation at 1000 °C, see Fig. 4. It is seen that the protrusion height increases with both initial oxide thickness and second oxide thickness. For an initial oxide thickness of 357 nm, corresponding to the experimental value, the protrusion height has been simulated, showing excellent agreement over a large range of second oxide thicknesses, thereby confirming the validity of the model.

B. Array Fabrication

In Fig. 5, the result of the double oxidation process (left) and proposed process (right) is shown in split-screen view. It is clearly visible that the 2 µm top plate on most of the arrays to the left have broken off due to poor bonding, resulting in a yield of 7 %. As opposed to this, all arrays are bonded flawlessly for the proposed fabrication process with SiO_2/SiO_2 bonding seen to the right, corresponding to 100 % yield. Martini et al. investigated the crack length of the unbonded region for step heights from 9 nm to 400 nm [7]. For step heights above 55 nm, thin plate theory could be used to predict the crack length. For step heights lower than 55 nm, i.e. in the regime of the protrusion heights seen in this study, dislocation theory was seen to provide a better description, with the crack length L being given by $L = Eh^2/[8\pi\gamma(1-\nu)^2]$. Here, E is the Young's modulus and ν the Poisson ratio of the bonded wafers, while h is the protrusion height and γ is the surface energy of the bonding surfaces. For the anisotropic stiffness properties of the silicon wafers bonded in this study, an average Young's modulus of 148 GPa and a Poisson ratio of 0.177 represent appropriate values. Assuming a representative fracture surface energy of 0.1 J/m^2, a protrusion height of 30 nm would result in a crack length of $\sim$ 80 µm. Even for the smallest measured protrusion height of 11 nm, the crack length would be $\sim$ 10 µm. Two neighboring cavities will therefore need an interdistance well above 20 µm to ensure even a small bonded area between the cavities. In the fabricated arrays, the interdistance was 20 µm, and the fact that the double oxidized wafers did not bond corresponds well to this theoretical prediction. Note that the fracture surface energy used in the calculation corresponds to the typical fracture surface energy before annealing [4]. Annealing will contribute to an increase in fracture surface energy up to a factor of 10 or more by conversion of hydrogen bonds to covalent bonds [4]. However, since completely non-bonded regions between cavities will not close during annealing, the pre-annealing fracture surface energy is the appropriate measure.

The interdistance between cavities in a CMUT array should be kept at a minimum, while still maintaining the required mechanical stiffness, to maximize the fill-factor and hence the highest possible output and sensitivity of the array [8]. Clearly, the double oxidation approach counteracts this. Etching or polishing steps performed prior to the bonding can be used to reduce the protrusions [2], but the issue can be completely bypassed without any additional steps by using the process proposed in this paper, which furthermore contributes with a slightly increased insulation thickness between the electrodes compared to the double oxidation process, see Figs. 1a and 1b. The only requirement is that the reduction of the SOI device layer thickness due to the oxidation is considered in the design.

IV. Conclusion

The protrusions arising from a double oxidation process was investigated using AFM measurements, numerical simulations and a proposed analytical model showing good agreement with simulations, proving that protrusions arise purely due to geometrically dependent diffusion. It was found that the protrusion height increases slightly with temperature, and that the protrusions from isotropically wet etched cavities are significantly smaller than protrusions from anisotropically wet etched cavities. In all cases, it was found that direct wafer bonding would be severely affected by the protrusions for a typical CMUT array using processing parameters in the investigated range. This fact was examplified through fabrication of representative CMUT arrays on a 4" wafer, demonstrating poor bonding equivalent to a 7 % yield. A simple process requiring no additional processing steps was proposed to completely remove the problem of protrusions, and a demonstration of the process revealed void-free wafer bonding resulting in 100 % yield.

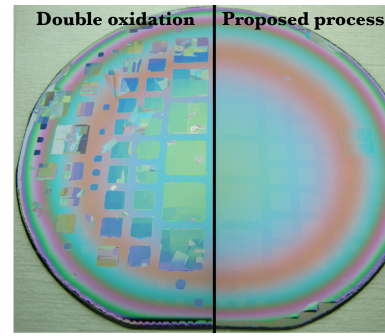

Fig. 5: A split-screen view of the result of the array fabrication using the double oxidation process (left) and the process proposed in this paper (right), showing poor and excellent bonding results, respectively. The color variation is due to variations in BOX layer thickness after the handle removal.

Acknowledgment

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